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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,174	02/13/2004	Kenneth Koch II	10017911-3	4476

7590 03/23/2006

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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,174	KOCH ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,7-12,14,16-18 and 20-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,7-12,20,21 and 23-26* is/are rejected.

7)☒ Claim(s) *14,16-18 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/2/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 7-12, 14, 16-18 and 20-26 are objected to because of the following informalities:

Claim 7, line 4, "can flow" should be changed to --flows-- because "can" is not a positive recitation of the invention.

Claims 8-12, 25 and 26 are objected to because they include the informality of claim 7.

Also, in claim 11, the recitations "PFETs" on line 3 and "NFETs" on line 4 should be changed to --PFET-- and --NFET--, respectively.

Claim 14, lines 27 and 32, --further-- should be inserted before "comprising".

Claims 16-18 and 22 are objected to because they include the informalities of claim 14.

Claim 20, line 12, --further-- should be inserted before "including".

Claim 20, line 17, --further-- should be inserted before "comprising".

Claim 21 and 23 are objected to because they include the informalities of claim 20.

Also, in claim 22, line 8, "the first resistive" should be changed to --the second resistive-- to avoid misdescriptive problem since it is being for the second inverter.

Claim 24, line 20, "can flow" should be changed to --flows-- because "can" is not a positive recitation of the invention.

Claim 24, line 18, --further-- should be inserted before "including".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 11, 12 and 24-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 11, the recitation "wherein the inverter includes a PFET and an NFET" causes the claim to be indefinite because it is not clear if the inverter includes the PFET and NFET (recited in claim 11) in addition to the field effect transistor recited earlier (see claim 8), i.e., it is not clear if the field effect transistors of the inverter comprises a PFET and an NFET, or the inverter comprises the field effect transistors (claim 8) and further comprises a PFET and an NFET. Clarification and/or appropriate correction is requested.

Further, in claim 11, the recitation "of each of the inverters" on line 5 is indefinite because "the inverters" lacks antecedent basis and it is not clear where the inverters come from. Note that the claim, so far, recites only one inverter (i.e., "an inverter" recited in claim 8). Clarification and/or appropriate correction is requested.

Claims 12, 25 and 26 are indefinite because they include the indefiniteness of claim 11.

With respect to claim 24, the recitation "wherein the inverter includes a PFET and an NFET" on lines 25-26 causes the claim to be indefinite because it is not clear if the inverter includes the PFET and NFET (recited on lines 25-26) in addition to the field effect transistor recited earlier (on line 23), i.e., it is not clear if the field effect transistors of the inverter comprises a PFET and an NFET, or the inverter comprises the field effect transistors and further comprises a PFET and an NFET. Clarification and/or appropriate correction is requested.

Also, in claim 24, the recitations "the NFET" (both occurrences on line 34) and "the PFET" (on line 35) are indefinite because it is not clear if the NFET and PFET recites on lines 34

and 35 are for the PFET and NFET of the first and second transistors of the driver, or whether they are the NFET and PFET of the inverter. Further, the recitation "substantial current flows through the resistor while the NFET is switched on and insubstantially current flows through the resistor while the NFET is switched on and the PFET is switched off" on the last 2 lines of the claim is indefinite because it is not clear whether the current is flown through the resistor or not when the NFET is switched on since the above recitation recites that substantial current flows through the resistor while the NFET is switched ON, and at the same time also recites that insubstantial current flows through the resistor while the NFET is switched OFF. Clarification and/or appropriate correction is requested.

Also, in claim 25, the recitation "wherein the resistor is connected between the source drain path of the PFET of the inverter and the output terminal of the inverter" is indefinite because it would be misdescriptive. Note that claim 1 clearly requires that first transistor of the driver being a PFET (see lines 3-4 of claim 1), and also requires that the resistive element (lines 11-13 of claim 1, note that the resistive element is the resistor as recited in claim 10) being connected for supplying current to the gate electrode of the first transistor (i.e., the PFET transistor of the driver which is recited on line 3-4 of claim 1). Thus, by recited that the resistor is connected between the source drain path of the PFET of the inverter and the output terminal of the inverter as in claim 25 causes the claim to be misdescriptive because it is inconsistent with what already claimed since Figure 1 clearly shows the resistor (46) connected between PFET (42) of the inverter and the output terminal of the inverter cannot supply current to the PFET 48 of the driver (as required in claim 1, lines 11-13 that the resistive element being connected for

supplying current to the gate electrode of the first transistor). Clarification and/or appropriate correction is required.

Claim 26 is indefinite because it includes the indefiniteness of claim 25.

Also, in claim 26, the recitations "the PFET" (on line 4 and 5) and "the PFET" (on line 5) are indefinite because it is not clear if the PFET and NFET recites on lines 34 and 35 are for the PFET and NFET of the first and second transistors of the driver, or whether they are the PFET and NFET of the inverter. Further, the recitation "substantial current flows through the resistor while the PFET is switched on and insubstantially current flows through the resistor while the PFET is switched on and the NFET is switched off" on the last 2 lines of the claim is indefinite because it is not clear whether the current is flown through the resistor or not when the PFET is switched on since the above recitation recites that substantial current flows through the resistor while the PFET is switched ON, and at the same time also recites that insubstantial current flows through the resistor while the PFET is switched OFF. Clarification and/or appropriate correction is requested.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3, 7 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Love (USP 5,068,553).

With respect to claims 1 and 3, Figure 3 of Love discloses a circuit which includes a first terminal (IN); a driver (86, 88) having a first transistor (PFET 86) and a second transistor (NFEF 88); output terminal (OUT); opposite power supply terminals Vdd and Ground (note that a first power supply terminal of the power supply terminals is Ground); pulse shaping circuitry (68, 72, 70 and 80) comprising a resistive element (any combination of 68, 72 and/or 70) and a capacitor (NFET 80). Note that because the PFET and NFET transistors having opposite conductivity so the on/off of transistors 86 and 88 in Figure 3 must be opposite to each other, i.e., transistors 86 and 88 are not ON simultaneously (i.e., when input IN is Hi then node 76 is Lo, then transistor 86 is ON so the source-drain path of transistor 86 is ON, while transistor 88 is OFF which is the source-drain path of the transistor 88 is OFF; and vice versa, when input IN is LO, so node 76 is Hi, then source-drain path of transistor 86 is OFF while source-drain path of transistor 88 is ON). Note that "one of said transistors" is the PFET transistor 86, and the other of the transistors is the NFET transistor 88; and thus the capacitor (NFET 80) comprises an FET having a conductivity type opposite to the conductivity type of the one of the transistors (PFET 86).

With respect to claim 7, Figure 3 shows the pulse shaping circuitry (68, 72, 70, 80) comprises a switching circuit (68, 72, 70) having an input terminal (62) and an output terminal (76) that is connected so current flows via a DC path between (a) the first power supply terminal (Ground) and (b) the capacitor (80) and the gate electrode of the one transistor (PFET 86), the DC path includes the resistive element (70).

With respect to claim 8, Figure 3 shows a switching circuit (68, 72, 70) comprises an inverter.

Claim Rejections – 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3, 7-12, 20, 21 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bui et al. (USP 6,201,752) in view of Wanlass (USP 3,356,858).

Note that Figure 8A discloses a circuit, which includes: a first terminal (801) for receiving a voltage source (IN); a driver (inverter 809); an output terminal (810); and circuitry (802, 803, 805, 806, 807, 808). The Bui et al. reference does not discloses that the inverter 809 comprise a PFET and an NFET. However, the Wanlass reference discloses in Figure 5 that an inverter is easily formed by using a PFET connected with an NFET transistor that provides advantage such as low power consumption. Therefore, it would have been obvious to one having skill in the art at the time the invention was made to modify the circuit in Figure 8A of Bui et al. by using the inverter having a PFET and an NFET as taught in Figure 5 of Wanlass for the inverter 809 (Figure 8A, Bui et al.) for the purpose of reduce power consumption. Thus, this modification/combination meets all the limitations of the above claims as specifically discussed below.

With respect to claims 1 and 3, the modification of Figure 8A of Bui et al. as discussed above discloses a circuit which includes a first terminal (IN); a driver (PFET and NFET inside of inverter 809) having a first transistor (PFET) and a second transistor (NFEF); output terminal (OUT); opposite power supply terminals (power supply Vdd and Ground, note that a first power

supply terminal of the power supply terminals is Ground); pulse shaping circuitry (802, 803, 805, 806, 807, 808) comprising a resistive element (805) and a capacitor (NFET 808). Note that because the PFET and NFET transistors having opposite conductivity so the on/off of the PFET and NFET transistors inside inverter 809 must be opposite to each other, i.e., the PFET and NFET inside inverter 809 are not ON simultaneously (i.e., when input IN is Hi then node 804 is Lo, then PFET transistor inside 809 is ON so the source-drain path of PFET transistor inside 809 is ON, while NFET inside 809 is OFF which is the source-drain path of the NFET inside 809 is OFF; and vice versa, when input IN is LO, so node 804 is Hi, then source-drain path of PFET inside 809 is OFF while source-drain path of NFET inside 809 is ON). Note that "one of said transistors" is the PFET transistor inside 809, and the other of the transistors is the NFET transistor inside 809; and thus the capacitor (NFET 808) comprises an FET having a conductivity type opposite to the conductivity type of the one of the transistors (PFET inside 809).

With respect to claim 7, Figure 8A shows the pulse shaping circuitry (802, 803, 805, 806, 807, 808) comprises a switching circuit (802, 803, 805, 806) having an input terminal (801) and an output terminal (804) that is connected so current flows via a DC path between (a) the first power supply terminal (Ground) and (b) the capacitor (808) and the gate electrode of the one transistor (PFET inside 809), the DC path includes the resistive element (805).

With respect to claims 8-12, Figure 8A shows a switching circuit (802, 803, 805, 806) comprises an inverter. Note that the inverter comprises a PFET (802), an NFET (806) and the resistor (805) connected between the source drain path of the NFET (806) of the inverter and the output terminal (804) of the inverter.

With respect to claims 20, 21 and 23, the modification of Figure 8A of Bui et al. as discussed above discloses a circuit which includes a first terminal (IN); a driver (PFET and NFET inside of inverter 809) having a first transistor (PFET); output terminal (OUT); first (ground) and second (power Vdd) opposite power supply terminals; pulse shaping circuitry (802, 803, 805, 806, 807, 808) comprising: a switching circuitry (802, 803, 805, 806) including an output terminal (804) that is DC connected to the control electrode of the first transistor (PFET inside 809), and a capacitor (NFET 808) connected between the control electrode of the first transistor (PFET inside 809) and the first power supply terminal (ground), the switching circuitry (802, 803, 805, 806) further including a resistive element (resistor 805) and second and third transistors (802, 806) that is formed an inverter (802, 803, 805, 806), wherein the resistive element (805) is connected between the source-drain path of the third transistor (806) and the output terminal (804) of the inverter.

Insofar as understood in claim 24, the modification of Figure 8A of Bui et al. as discussed above discloses a circuit which includes a first terminal (IN); a driver (PFET and NFET inside of inverter 809) having a first transistor (PFET) and a second transistor (NFEF); output terminal (OUT); opposite power supply terminals (power supply Vdd and Ground, note that a first power supply terminal of the power supply terminals is Ground); pulse shaping circuitry (802, 803, 805, 806, 807, 808) comprising a resistive element (805) and a capacitor (NFET 808). Note that because the PFET and NFET transistors having opposite conductivity so the on/off of the PFET and NFET transistors inside inverter 809 must be opposite to each other, i.e., the PFET and NFET inside inverter 809 are not ON simultaneously (i.e., when input IN is Hi then node 804 is Lo, then PFET transistor inside 809 is ON so the source-drain path of PFET transistor inside 809

is ON, while NFET inside 809 is OFF which is the source-drain path of the NFET inside 809 is OFF; and vice versa, when input IN is LO, so node 804 is Hi, then source-drain path of PFET inside 809 is OFF while source-drain path of NFET inside 809 is ON). Note that "one of said transistors" is the PFET transistor inside 809, and the other of the transistors is the NFET transistor inside 809; and thus the capacitor (NFET 808) comprises an FET having a conductivity type opposite to the conductivity type of the one of the transistors (PFET inside 809). Note that Figure 8A shows the pulse shaping circuitry (802, 803, 805, 806, 807, 808) comprises a switching circuit (802, 803, 805, 806) having an input terminal (801) and an output terminal (804) that is connected so current flows via a DC path between (a) the first power supply terminal (Ground) and (b) the capacitor (808) and the gate electrode of the one transistor (PFET inside 809), the DC path includes the resistive element (805); and Figure 8A also shows that switching circuit (802, 803, 805, 806) comprises an inverter wherein the inverter comprises a PFET (802), an NFET (806) and the resistor (805) connected between the source drain path of the NFET (806) of the inverter and the output terminal (804) of the inverter.

Insofar as understood in claims 25 and 26, the modification of Figure 8A of Bui et al. as discussed above discloses a circuit which includes a first terminal (IN); a driver (PFET and NFET inside of inverter 809) comprises a PFET and an NFET; output terminal (OUT); opposite power supply terminals (power supply Vdd and Ground, note that a first power supply terminal of the power supply terminals is power Vdd); pulse shaping circuitry (802, 803, 805, 806, 807, 808) comprising a resistive element (803) and a capacitor (PFET 807). Note that because the PFET and NFET transistors having opposite conductivity so the on/off of the PFET and NFET transistors inside inverter 809 must be opposite to each other, i.e., the PFET and NFET inside

inverter 809 are not ON simultaneously (i.e., when input IN is Hi then node 804 is Lo, then PFET transistor inside 809 is ON so the source-drain path of PFET transistor inside 809 is ON, while NFET inside 809 is OFF which is the source-drain path of the NFET inside 809 is OFF; and vice versa, when input IN is LO, so node 804 is Hi, then source-drain path of PFET inside 809 is OFF while source-drain path of NFET inside 809 is ON). Note that "one of said transistors" is the NFET transistor inside 809, and the other of the transistors is the PFET transistor inside 809; and thus the capacitor (PFET 807) comprises an FET having a conductivity type opposite to the conductivity type of the one of the transistors (NFET inside 809). Note that Figure 8A shows the pulse shaping circuitry (802, 803, 805, 806, 807, 808) comprises a switching circuit (802, 803, 805, 806) having an input terminal (801) and an output terminal (804) that is connected so current flows via a DC path between (a) the first power supply terminal (Vdd) and (b) the capacitor (807) and the gate electrode of the one transistor (NFET inside 809), the DC path includes the resistive element (803); and Figure 8A shows a switching circuit (802, 803, 805, 806) comprises an inverter (802, 803, 805, 806), wherein the inverter comprises a PFET (802), an NFET (806) and the resistor (803) connected between the source drain path of the PFET (802) of the inverter and the output terminal (804) of the inverter.

Allowable Subject Matter

8. Claims 14, 16-18 and 22 presently would be allowed if amend to overcome the informality set forth above.

Response to Arguments

9. Applicant's arguments have been fully considered but are moot in view of the new ground(s) of rejection.

Note, applicant argues that "if ground of Love is considered to be the first power supply terminal, the "other" transistor of claim 1 must be considered as NFET 88 of Love. However, NFET 88 of Love has the same conductivity type as NFET 80 of Love that forms the capacitor between the gate of NFET and ground. Hence, the interpretation of Love in this paragraph is not consistent with claim 1". However, this argument is not persuasive because claim 1 requires that the capacitor comprising an FET having a conductivity type opposite to the conductivity type of said one of said transistors (i.e., not the other of the transistors), so the interpretation of Love is consistent with claim 1. Note that, with regard to the Love reference, the above rejection clearly discussed a first power supply terminal of the power supply terminals is Ground; a capacitor (NFET 80); "one of said transistors" is the PFET transistor 86, and the other of the transistors is the NFET transistor 88; and thus the capacitor (NFET 80) comprises an FET having a conductivity type opposite to the conductivity type of the one of the transistors (PFET 86).

With respect to applicant's argument regarding the transistors not turn on simultaneously. It is further note that, as discussed in the above rejection, because the PFET and NFET transistors having opposite conductivity so the on/off of transistors 86 and 88 in Figure 3 must be opposite to each other, i.e., transistors 86 and 88 are not ON simultaneously (i.e., when input IN is Hi then node 76 is Lo, then transistor 86 is ON so the source-drain path of transistor 86 is ON, while transistor 88 is OFF which is the source-drain path of the transistor 88 is OFF; and vice versa, when input IN is LO, so node 76 is Hi, then source-drain path of transistor 86 is OFF while source-drain path of transistor 88 is ON).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LONG NGUYEN
PRIMARY EXAMINER